

	Document ID	Issue Date	Pag es	Title	Current OR
1	US 20060056620 A1	20060316	46	Processes, circuits, devices, and systems for encryption and decryption and other purposes, and processes of making	380/28
2	US 20060045294 A1	20060302	77	Personalized headphone virtualization	381/309
3	US 20050254106 A9	20051117	252	Scanning device for coded data	358/539
4	US 20050089101 A1	20050428	22	Sub-block domain transformation multiple signal processing	375/240.18
5	US 20050052556 A1	20050310	126	Image processor	348/308
6	US 20050046718 A1	20050303	126	Image sensor timing circuit	348/308
7	US 20050046717 A1	20050303	126	Synchronization protocol	348/308
8	US 20050036039 A1	20050217	127	Image sensor with range expander	348/222.1
9	US 20050024524 A1	20050203	127	Image processor with low power mode	348/372
10	US 20050024512 A1	20050203	127	Pixel sensor	348/294
11	US 20050024511 A1	20050203	127	Image sensor with low-pass filter	348/294
12	US 20050024510 A1	20050203	126	Image sensor with digital frame store	348/294
13	US 20040213358 A1	20041028	30	Radio receiver for receiving both VSB and QAM digital HDTV signals	375/316
14	US 20040190092 A1	20040930	244	Scanning device for coded data	358/539
15	US 20040190085 A1	20040930	255	Sensing device for coded data	358/474
16	US 20030193618 A1	20031016	30	RADIO RECEIVER FOR RECEIVING BOTH VSB AND QAM DIGITAL HDTV SIGNALS	348/729
17	US 20030032402 A1	20030213	39	Analog signal control method, analog signal controller, and automatic gain controller	455/234.1

	Current XRef	Inventor
1		Shingal; Tonmoy et al.
2	381/74	Smyth; Stephen Malcolm
3	358/474	Silverbrook, Kia et al.
4		Tellado, Jose et al.
5		Henderson, Peter Charles Boyd et al.
6		Yourlo, Zhenya Alexander et al.
7		Lapstun, Paul et al.
8		Silverbrook, Kia et al.
9		Yourlo, Zhenya Alexander et al.
10		Moini, Alireza et al.
11		Lapstun, Paul et al.
12		Lapstun, Paul et al.
13	348/726	Patel, Chandrakant Bhailalbhai et al.
14	358/474	Silverbrook, Kia et al.
15	358/539	Silverbrook, Kia et al.
16	348/731; 375/321	PATEL, CHANDRAKANT BHAILALBHAI et al.
17	375/344	Asano, Shigetaka

	Document ID	Issue Date	Pag es	Title	Current OR
18	US 20010041012 A1	20011115	13	Parallel data processing	382/234
19	US 7046746 B1	20060516	15	Adaptive Viterbi decoder for a wireless data network receiver	375/341
20	US 6738205 B1	20040518	49	Self-writing of servo patterns in disk drives	360/17
21	US 6252464 B1	20010626	32	Numerically-controlled nyquist-boundary hopping frequency synthesizer	331/4
22	US 6222478 B1	20010424	9	Pipeline analog-to-digital conversion system using a modified coding scheme and method of operation	341/162
23	US 5961580 A	19991005	21	Apparatus and method for efficiently calculating a linear address in a microprocessor	708/670
24	US 5960467 A	19990928	27	Apparatus for efficiently providing memory operands for instructions	711/214
25	US 5867723 A	19990202	62	Advanced massively parallel computer with a secondary storage device coupled through a secondary storage interface	712/11
26	US 5835968 A	19981110	26	Apparatus for providing memory and register operands concurrently to functional units	711/214
27	US 5813045 A	19980922	21	Conditional early data address generation mechanism for a microprocessor	711/204
28	US 5808573 A	19980915	30	Methods and structure for sampled-data timing recovery with reduced complexity and latency	341/110

	Current XRef	Inventor
18	375/240.2; 375/240.2 9	Hsieh, Jeff et al.
19	375/265; 714/795	Keaney; Richard A. et al.
20	360/75	Moran; Patrick et al.
21	327/107; 331/178; 331/25; 375/376; 708/271	Richards; Wayne Edward et al.
22	341/155	Bright; William J.
23	711/220	Mahalingaiah; Rupaka
24	711/212; 711/213; 711/215	Mahalingaiah; Rupaka et al.
25	711/114; 711/119; 712/13; 712/20	Chin; Danny et al.
26	711/212; 711/213; 711/215; 712/230	Mahalingaiah; Rupaka et al.
27	711/202; 711/213; 711/214; 711/215; 712/207; 712/211	Mahalingaiah; Rupaka et al.
28	341/159	Shih; Shih-Ming et al.